Infineon

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Memory Products

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Infineon technologies

Never stop thinking.

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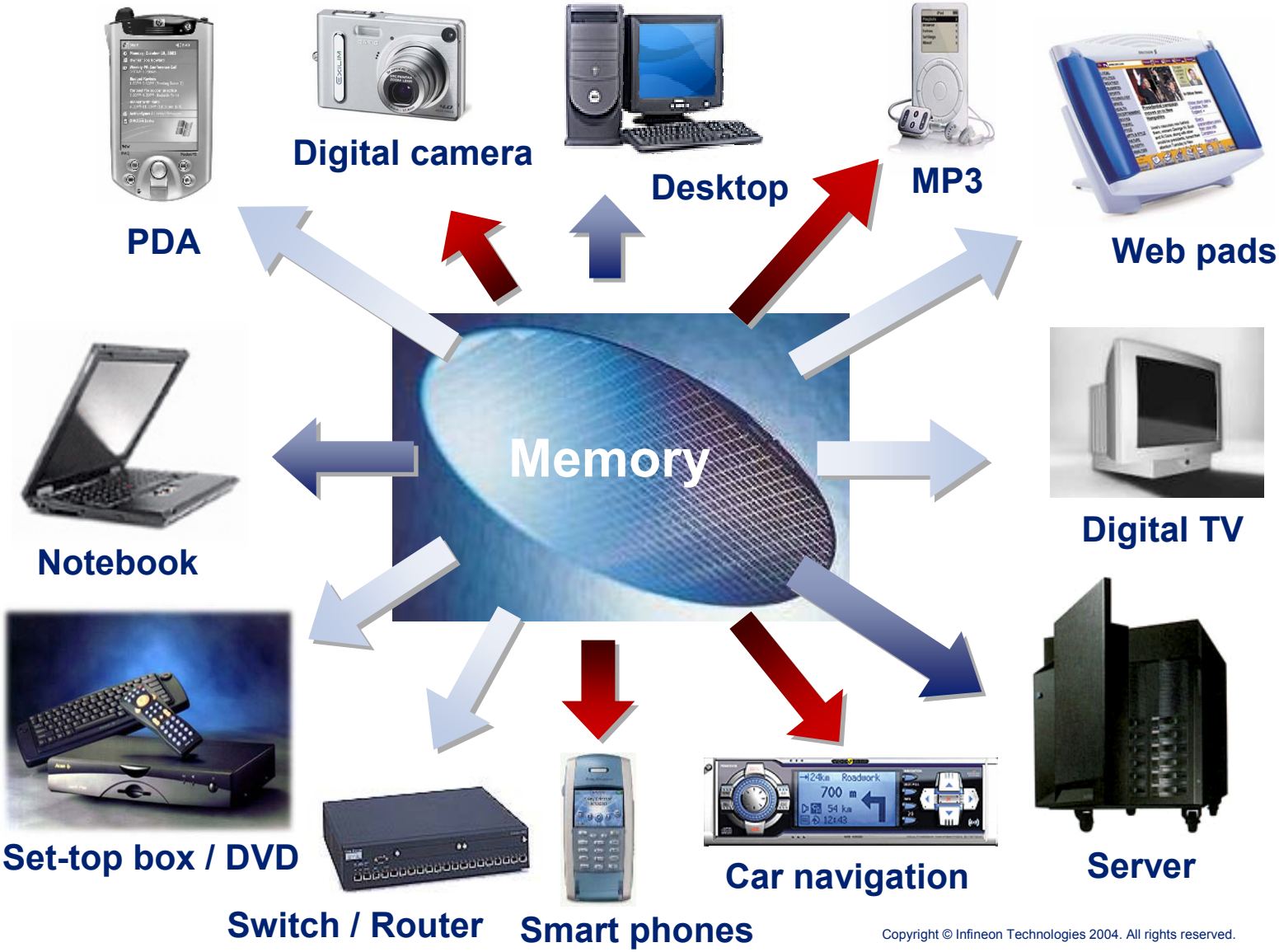
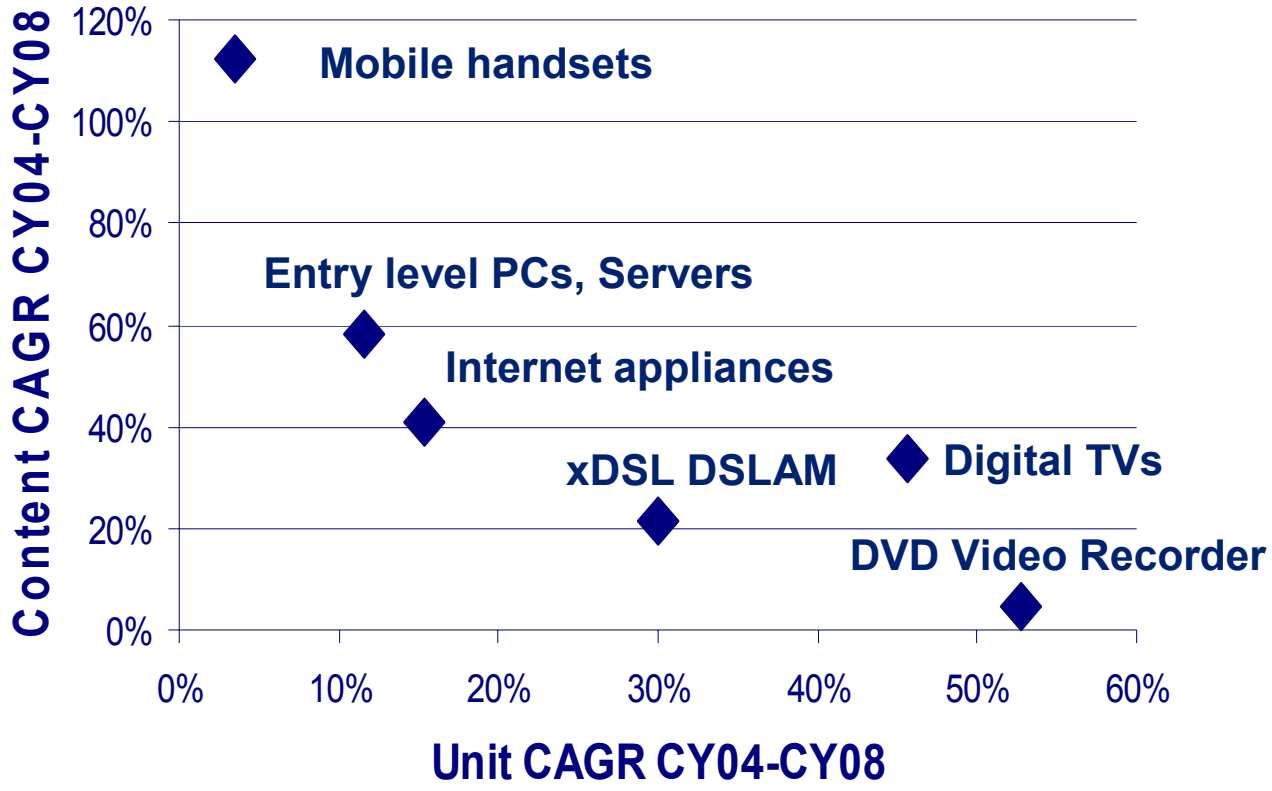
The universe of memory applications is expanding



Opening up a range of growth and value opportunities



Top DRAM supplier's challenge is the right mix of:

⇨ Volume products for computing segment

⇨ Innovative products for leading-edge applications

⇨ Legacy or standard products for upcoming consumer demand

* Source: iSuppli, Q3 2004

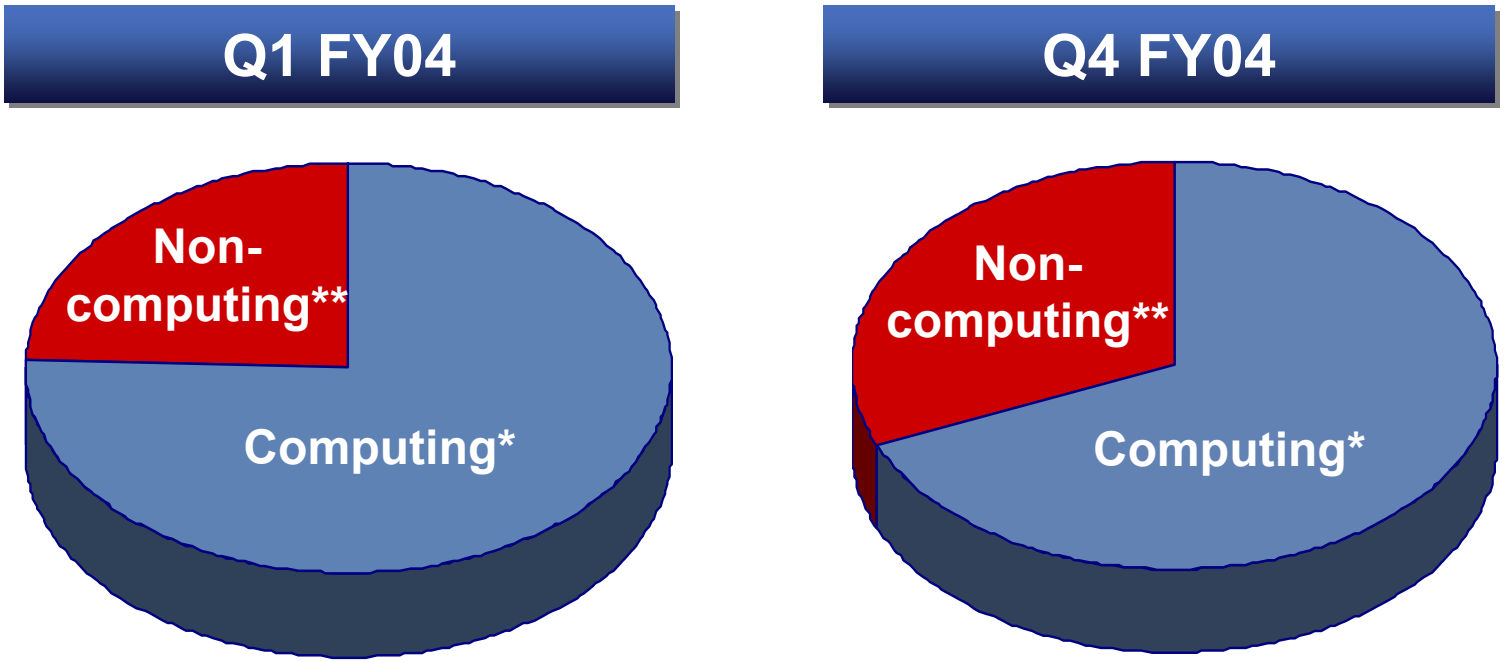
Agenda

- Focus on higher margin segments
- Technology leadership
- Strong partnership network

Focus on higher margin segments

- **Application-specific integration and innovation**
  - Broaden module portfolio for infrastructure and mobile PCs
  - Increase bit-share of specialty DRAMs
- **Consumer niches with strong growth potential**
  - Check mainstream product supply for consumer segment
  - Extend SDRAM product portfolio
- **Market-enabling and cross-selling opportunities**
  - Close cooperation with market enablers for future DRAM generations
  - Use other segments' expertise to introduce innovative memory products such as fully-buffered DIMMs

Bit shipment share of non-computing applications increased to more than 30% in Q4 FY04



* Desktop PCs, Notebooks and Workstations; ** Infrastructure, Consumer, Mobile Applications

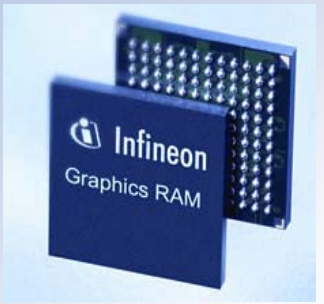
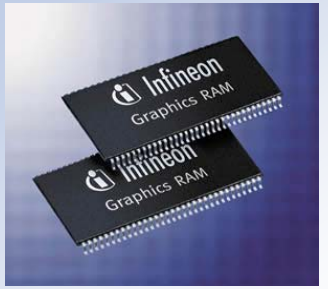
- ⇨ A leading supplier to server manufacturers
- ⇨ Leading with Mobile-RAMs
- ⇨ Increasing shipments of Graphics RAM
- ⇨ Increasing share of shipments for set-top boxes

Mobile-RAM: Low power for mobile applications

Portfolio	Features	Target applications
	**Small form factor** ⇨ **BGA package** **Low operating current** ⇨ **Up to 60% less than 3.3V SDRAM "low power sort"** **Low standby current** ⇨ **Up to 80% less than 3.3V SDRAM "low power sort"** **Low core voltage** ⇨ **Down to 1.8V**	 **- Smart Phone - PDA** **- Feature Phone - MP3** **- Digital Camera**

Densities: 128M – 512M
Speed: 133 MHz, CL3

Graphics RAM – Performance for desktop and notebook

Graphics segment	Features	Products
High end	High speed: 400 – 500 MHz BGA package Interface width: x32 Low operating current ⇨ 1.8V (notebook) ⇨ 2.0V (desktop)	 256M GDDR3
Mainstream	Mainstream speed: 200 – 250 MHz TSOP package Interface width: x16 Operating voltage 2.5V	 256M DDR
Value		

Upcoming fully-buffered DIMMs:
Take advantage of Infineon's unique in-house skill set

Memory Products

DRAM
Server module

Wireline

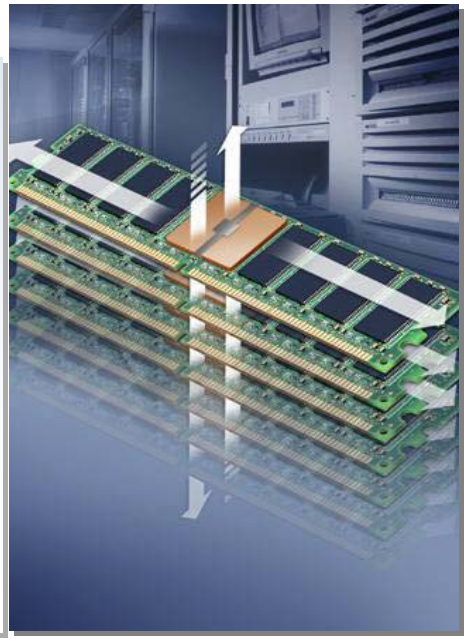
Buffer chip
Advanced memory buffer

New bus topology:

The parallel multi-drop bus is replaced by serial point-to-point connections

⇨ Allows larger number of DRAM modules per bus

Standard setting and market enabling done together with **Intel at JEDEC**



Features:

- Densities: 256MB – 4GB
- Point-to-point connection
- Buffer with up to 6 Gb/s transfer rate per pin

Market expectations:

- 35% share of server modules in 2006*
- 70% share in 2007*

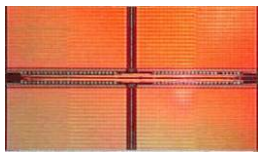
* Source: Infineon

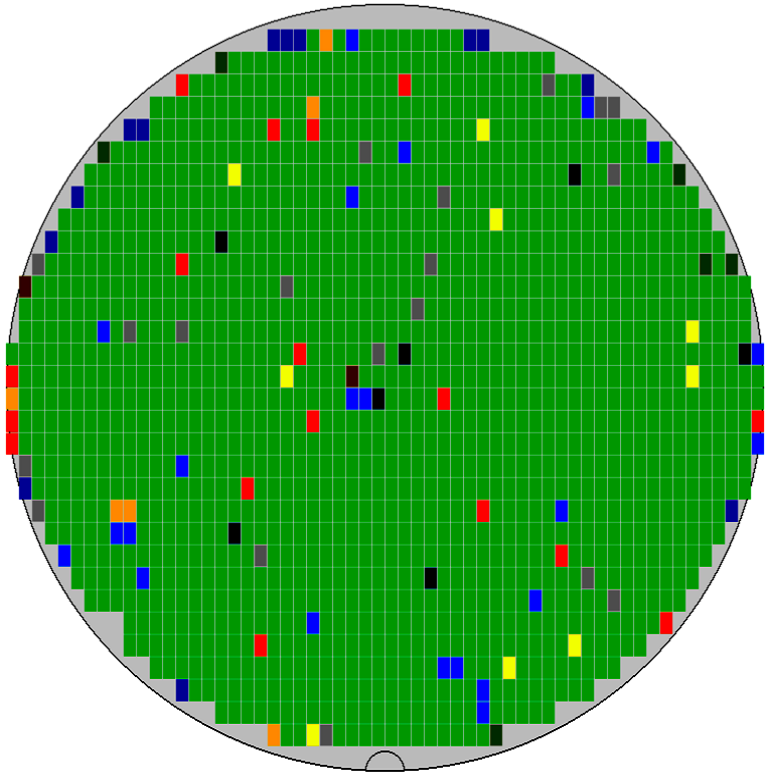
Agenda

- Focus on higher margin segments
- **Technology leadership**
- Strong partnership network

110nm technology in volume production

- Best wafer yield > 93.9%
- Know-how in 193nm litho extended
- All process parameters well established
- More than 80% of all capacities converted to 110nm by end FY04

Node	Status
110nm	Mass production  256M DDR 110nm



Green: Fully functional
Other: Various defects

110nm: Basis for global 300mm ramp-up in 2005

Winbond
Taiwan

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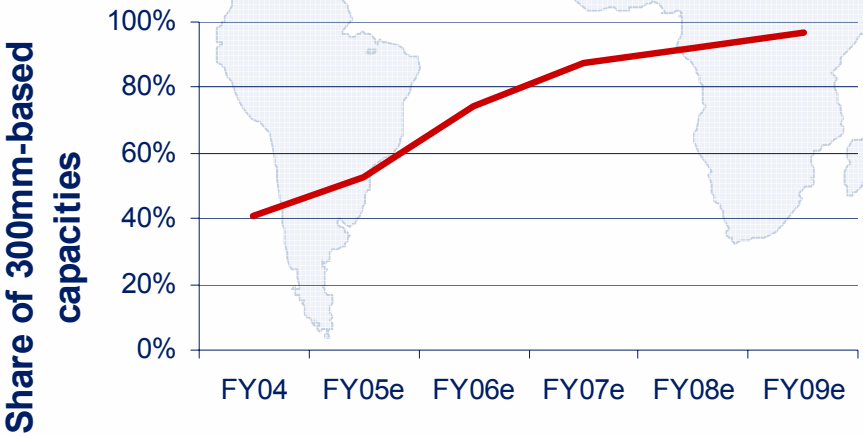
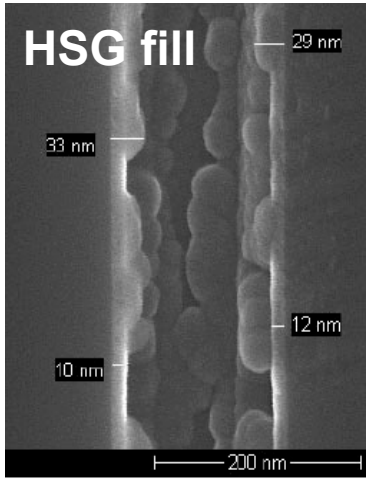


90nm technology functional

Key innovations:

- New cell layout
- Trench with HSG fill
- Bottle-shaped trench

Node	Status
110nm	Mass production
90nm	Customer samples from 200mm line
	Transfer to 300mm line started
	Ramp-up expected to start mid 2005
	 512M DDR 90nm



Bottle-shaped trench

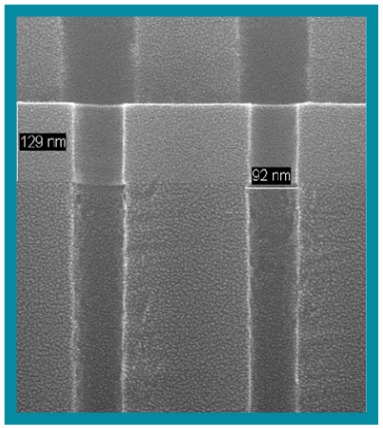
First demonstrators for 70nm produced

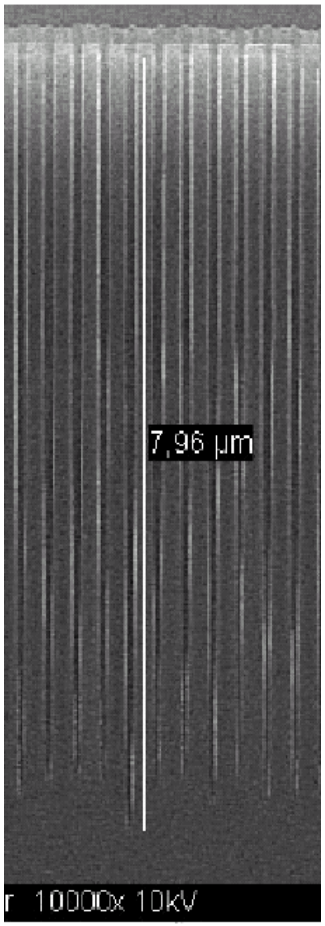
Key innovation:

- High-κ fill in trench

Node	Status
110nm	Mass production
90nm	Customer samples from 200mm line
70nm	First demonstrators on 300mm line

512M DDR2
70nm





High aspect-ratio etch

Agenda

- Focus on higher margin segments
- Technology leadership
- **Strong partnership network**

MP's partnership strategy

- **Generate mutual benefits**
  - Share risks but also opportunities: Margin-sharing principle
  - Improve economy of scale for manufacturing and development
- **Reduce risks**
  - Significant capital expenditure savings
  - Restricted licenses or limited technology transfer for partners that do not participate in technology development
  - Semiconductor technologies are outdated fast, and without special know-how, they are very hard to evolve
- **Relationship management**
  - A core competency of MP
  - MP has a long track record of successful partnerships

MP's alliances: Share risks and benefits and optimize economies of scale

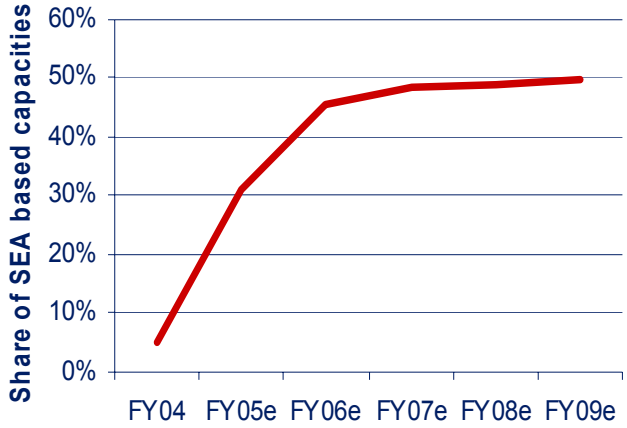
MP alliance model today

Joint development partnerships	Manufacturing partnerships
Secure mask technology development	Production of worldwide leading edge masks
Co-development of 90nm and 70nm DRAM technology	Joint manufacturing in Taiwan using 300mm technology
Joint venture with Saifun on flash memory business	Infineon Flash Development and production of data flash and code flash
Joint development of specialty DRAM products	License 110nm and 90nm DRAM technology in exchange for capacity
Development of MRAM	Foundry agreements for 8" and 12" capacities

Add resources in South East Asia

Capacities in South East Asia

Based on the additional capacities from SMIC, Inotera and Winbond we plan to increase the share of capacities SEA from around 5% in the current fiscal year to up to 50% in FY07



Development center in Xi'an, China

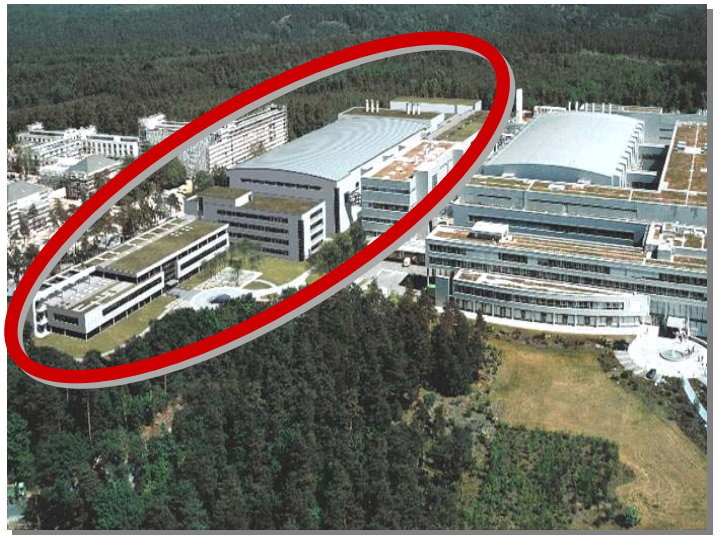
- More than 1,000 engineers planned by 2007
- Close cooperation with local universities for improved know-how transfer
- First product development activities started for memory products

Benefit through alliances with partners

- Investment of about USD 2.2 bn
- Capacity of 24,000 WSPM reached 2 months ahead of schedule in October 2004
- 300mm capacity of up to 54,000 WSPM by end of 2005
- First products: 256M DDR and 512M DDR2 in 110nm technology
- Largest DRAM manufacturing module worldwide when completed end of 2005

Memory development center in Dresden

- Approximately 400 employees including 50 from Nanya
- Technology: DRAM 90nm and 70nm
- Focusing development in 300mm line



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